What is claimed is:

1. A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device, the method comprising:

Controlling the conduction of an active discharging device, said active discharging device being coupled to said SOI device, whereby the parasitic bipolar transistor is deactivated.

2. The method of claim 1 further comprising:

providing a first signal to a first node of said SOI device;

providing a second signal to an input of said SOI device; and

activating the conduction of said active discharging device according to the state of said first and second signals.

3. The method of claim 2 wherein the first signal is a clock signal.

4. The method of claim 3 wherein said first node is charged high whenever said clock signal is active low.

5. The method of claim 2 wherein the second signal is an active low signal applied to said input during a pre-charge cycle.

6. The method according to claim 1, wherein the active discharging device provides a conduction path between said second node of SOI device and a common node.

7. A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) dynamic logic circuit having an input an output, a clock, a plurality of stacked SOI Metal Oxide Semiconductor (MOS) transistors interconnected to perform a predetermined logic function defining a common node and an intermediate node, said plurality of stacked SOI MOS transistors being controlled by a respective plurality of inputs, said common node being coupled to a pre-charging device and said intermediate node being in a path between said common node and a discharge potential, said path defined by said plurality of stacked SOI MOS transistors, said intermediate node being coupled to said common node by at least a first of said plurality of stacked SOI MOS transistors, and said intermediate node being coupled to said discharge potential by at least a second of said plurality of stacked SOI MOS transistors, and an active discharging transistor controlled by at least one of said plurality of inputs, said active discharging transistor defining a discharge path between said intermediate node and said discharge potential, the method comprising:

controlling the conduction of said active discharging transistor during a pre-charge cycle; and

actively discharging said intermediate nodes of the SOI stacked transistors, whereby the parasitic bipolar transistors are deactivated and the charge at said common

node is maintained at a predetermined level.

8. The method according to claim 7, wherein pre-charging occurs during a low state of said clock.

9. The method according to claim 7, wherein pre-charging occurs during a high state of said clock.

10. The method according to claim 7, wherein during the pre-charging all said inputs are set to a predetermined logic state.

11. The method according to claim 10, wherein said logic state is low.

12. The method according to claim 10, wherein said logic state is high.

13. The method according to claim 7, wherein the step of actively discharging said intermediate nodes prevents the body voltages of said stacked SOI transistors from reaching a voltage stage sufficient to activate the parasitic bipolar transistors of said stacked SOI transistors.

14. The method according to claim 7, wherein said stacked transistors are N-Field Effect Transistors (NFET) and said active discharging transistors are P-Field Effect Transistors (PFET).

15. The method according to claim 7, wherein said stacked transistors are P-Field Effect Transistors (PFET) and said active precharging transistors are N-Field Effect Transistors (NFET).

16. The method according to claim 7, wherein said pre-charging device comprises transistors coupled to said stacked transistors.